AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (canceled)

2. (previously presented) The semiconductor memory device according to claim 6, wherein said metal is a refractory metal, and said first contact further includes a barrier layer formed between said source and said first metal portion.

3. (previously presented) The semiconductor memory device according to claim 2, wherein said refractory metal is tungsten, and said barrier layer is formed of titanium nitride.

4. (original) The semiconductor memory device according to claim 3, wherein said bottom electrode includes:

a polysilicon layer connected to said dielectric layer, and

an electrode barrier layer formed between said first metal portion and said polysilicon layer.

5. (original) The semiconductor memory device according to claim 4, wherein said electrode barrier layer is formed of titanium nitride.

6. (currently amended) A semiconductor memory device comprising:

a substrate;

a MOS (metal oxide semiconductor) transistor formed in a surface portion of said substrate, wherein said MOS transistor includes a source, a gate, and a drain;

a first inter-level dielectric covering said MOS transistor;

a capacitor element including:

a bottom electrode,

a dielectric layer formed on said bottom electrode, and

an upper electrode formed on said dielectric layer;

a first contact formed through said first inter-level dielectric to electrically connect said bottom electrode to said source, wherein said first contact includes a first metal portion formed of metal; ~~and~~

a second contact formed through said first inter-level dielectric to be connected to said drain, wherein said second contact includes a second metal portion formed of said metal,

wherein said bottom electrode comprises a polysilicon layer connected to said dielectric layer, and an electrode barrier layer formed between said first metal portion and said polysilicon layer; and

a second inter-level dielectric covering said first inter-level dielectric, wherein a hole is formed through said second inter-level dielectric,

wherein said electrode barrier layer includes:

a bottom barrier portion formed on said metal portion of said first contact, and

a side barrier portion connected to said bottom barrier portion, said side barrier portion being formed on a side surface of said hole to extend towards an upper surface of said second inter-level dielectric,

wherein said polysilicon layer includes:

a bottom electrode portion formed on said bottom barrier portion, and

a side electrode portion connected to said bottom electrode portion, said side electrode portion being formed on said side barrier portion, and

wherein an end of said side electrode portion is substantially in alignment with said upper surface of said second inter-level dielectric, while an end of said side barrier portion is out of alignment with said upper surface of said second inter-

level dielectric, said side barrier portion not reaching said upper surface of said second inter-level dielectric.

7. (original) The semiconductor memory device according to claim 6, wherein said metal is tungsten, and said second contact further includes a second barrier layer formed of titanium nitride between said drain and said second metal portion.

8. (original) The semiconductor memory device according to claim 6, further comprising:

a second inter-level dielectric covering said capacitor element and said first inter-level dielectric;

a third contact formed through said second inter-level dielectric; and

a bit line formed on said second inter-level dielectric, wherein said second and third contact electrically connect said drain to said bit line.

9. (original) The semiconductor memory device according to claim 8, further comprising:

another MOS transistor provided in a surface portion of said substrate for a peripheral circuit;

a fourth contact formed through said first inter-level dielectric to be connected to said another MOS transistor on a source/drain thereof;

a fifth contact formed through said second inter-level dielectric to be connected to said fourth contact, wherein said fourth contact includes a third metal portion formed of said metal.

10. (canceled)

11. (currently amended) The semiconductor memory device according to claim [[10]] 6, wherein said electrode barrier layer is formed of titanium nitride.

12-22. (canceled)

23. (currently amended) A semiconductor memory device, comprising:

a substrate;

a transistor in a surface of said substrate, said transistor having a source, drain, and gate;

a first inter-level dielectric on said transistor;

a second inter-level dielectric on said first inter-level dielectric;

a capacitor element that extends through said second inter-level dielectric, said capacitor element having bottom and top electrodes and a capacitor dielectric therebetween;

a bit line contact plug that extends through said second inter-level dielectric;

a first contact through said first inter-level dielectric that connects said bottom electrode of said capacitor element to said source of said transistor; ~~and~~

a second contact through said first inter-level dielectric that connects said bit line contact plug to said drain of said transistor,

wherein said first and second contacts and said bit line contact plug are all formed of a same first metal; and

a barrier layer between said bottom electrode of said capacitor element and said second inter-level dielectric, said barrier layer extending only partially along said capacitor element so that a portion of said bottom electrode directly contacts said second inter-level dielectric.

24. (previously presented) The device of claim 23, wherein the first metal is tungsten.

25. (canceled)